

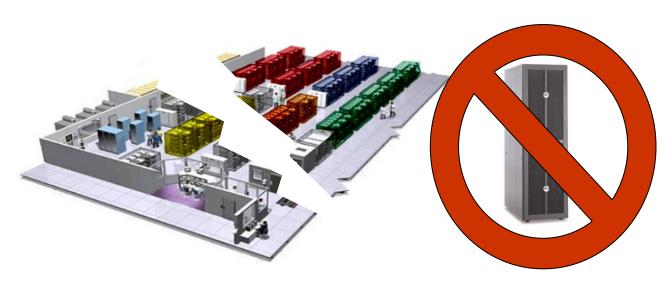
# Maximizing Data Center Efficiencies through Microprocessor Innovations

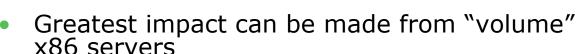
Ben Williams Vice President, Commercial Business Advanced Micro Devices

January, 31 2006

Conference on Enterprise Servers and Data Centers:
Opportunities for Energy Savings

### Stop the \$3,000,000 Server





- Innovations that contribute to a "Balanced Platform"
  - Performance-per-watt efficiencies
  - Manufacturing processes
  - Efficient microprocessor architectural



Cost to Build 50,000 ft<sup>2</sup> Data Center

1990's

40watts/sq.ft \$400/sq.ft \$20,000,000

1150%

500watts/sq.ft \$5,000/sq.ft

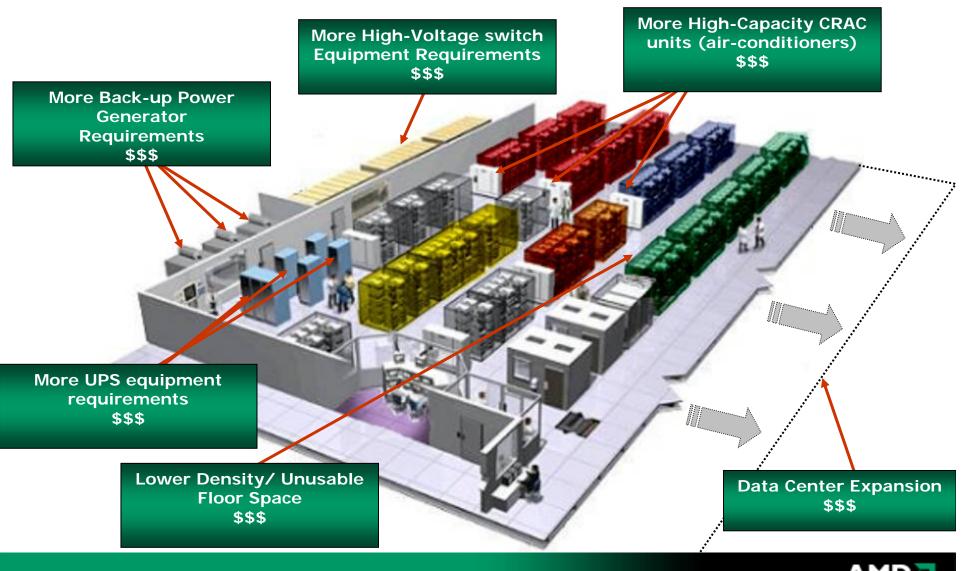
2010

\$250,000,000

Computerworld Nov.1 2004

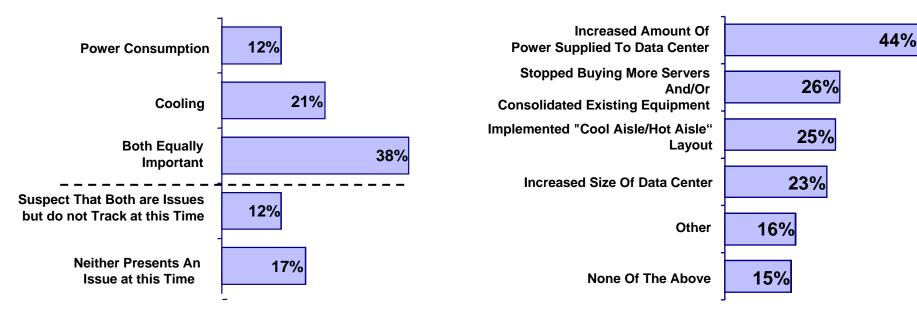


## Effects of Power in the Data Center It adds up quick!



#### IT Knows it has a Problem

Power Consumption/Cooling Issues Tracked By Company: 71% How Are Companies Addressing These Issues



Base: 1,177 IT Decision Makers November 2005

**Strategy Group/Ziff-Davis** 

Average of 18% of total rack space wasted due to power and cooling issues



Performance-per-watt Efficiencies It starts with the design

Efficient Cores

reducing the requirement to rely on frequency Get's more done per clock cycle

> Advanced Process Technology

Silicon-on-Insulator

Faster transistors with less power leakage

Reduces wasted power and heat

Integrated Memory Controller

<u>Decreases Power</u> by removing external memory controller requirement <u>up to ~48watts savings!</u>

AMD PowerNow!™ technology with Optimized Power Management

Dynamically reduces processor power based on workload up to 75% savings in power per processor!

Dual-Core native design

Increases performance-per-watt efficiencies <u>without increased</u> <u>power</u>

**Direct Connect Architecture** 

Provides faster I/O throughput

• I/O directly connected

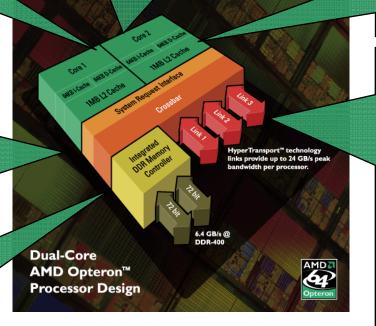
Provides <u>faster CPU-to-CPU</u> communication

CPUs directly connected

Integrated memory controller Increases performance by reducing memory latencies

• Memory directly connected

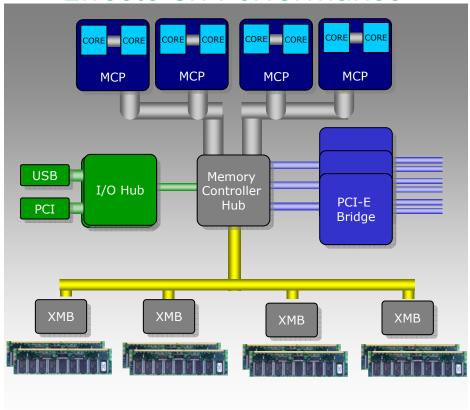
REMOVES THE LEGACY FRONT-SIDE BUS BOTTLENECKS





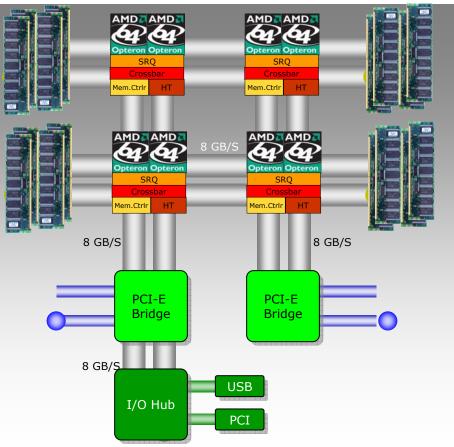
#### Designing a "Balanced" Architecture

Effects on Performance



#### **Traditional x86 Architecture**

- 20-year old front-side bus architecture
- CPUs, Memory, I/O all share a bus
- Major bottleneck to performance
- Faster CPUs or more cores ≠ performance

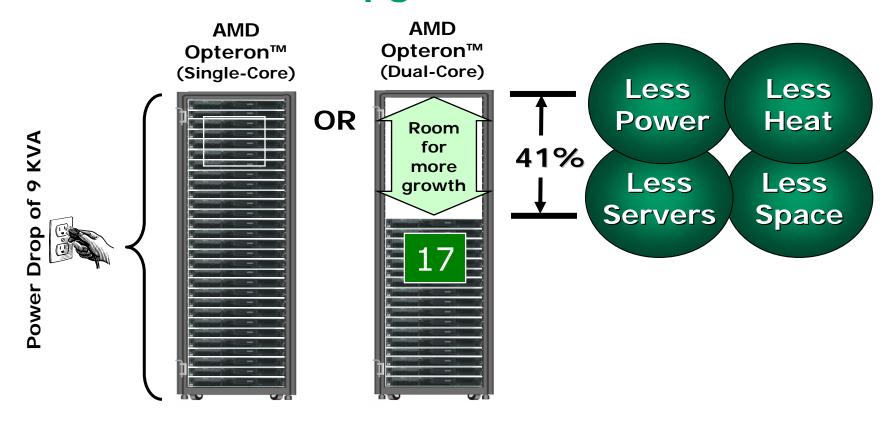


#### **AMD64's Direct Connect Architecture**

- Industry-standard AMD64 technology
- AMD's revolutionary Direct Connect Architecture eliminates the FSB bottleneck
- HyperTransport<sup>™</sup> technology interconnect for high bandwidth and low latency



## **Dual-Core - Increasing Performance** without Facilities Upgrades



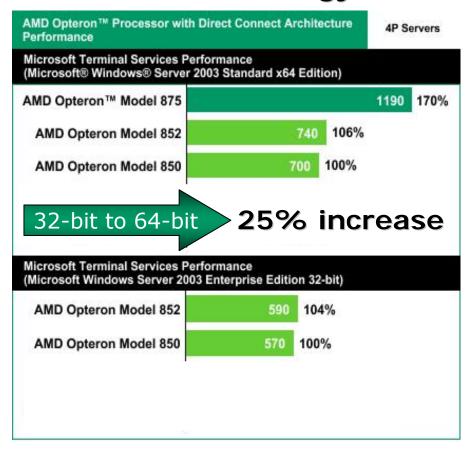
#### **Dual-Core Processors**

Increasing throughput within the same power and cooling envelope as single-core processors

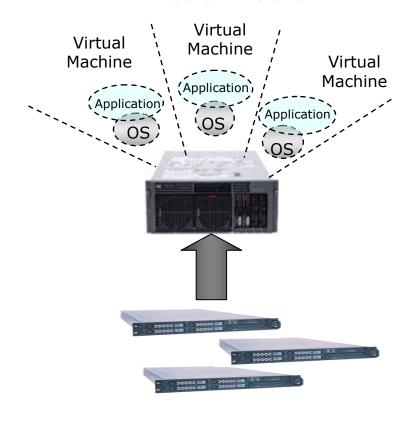


### Efficiency through Instruction Sets

#### 'AMD64 Technology'



#### 'Virtualization'

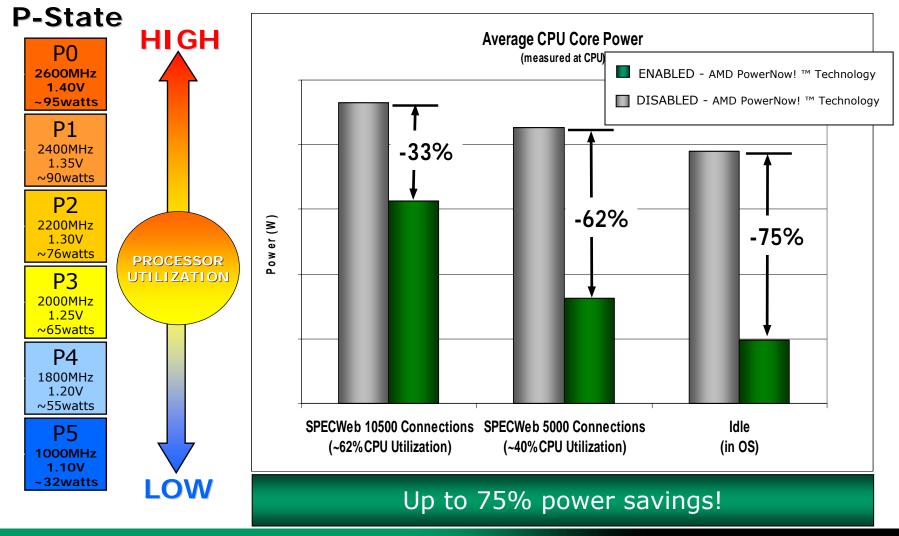


Getting more done without increased power and heat

Reduces number of power consuming servers

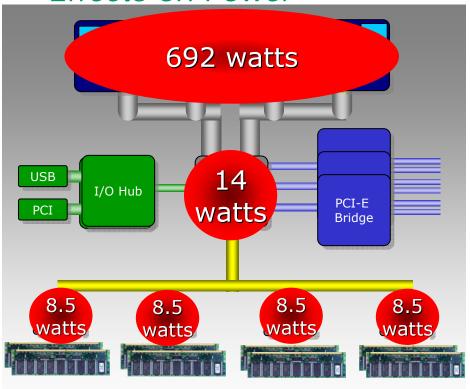


## Reducing Power and Cooling Requirements with Processor Performance States



### Significant Impacts via a "Balanced" Architecture

Effects on Power



#### **Traditional x86 Architecture**

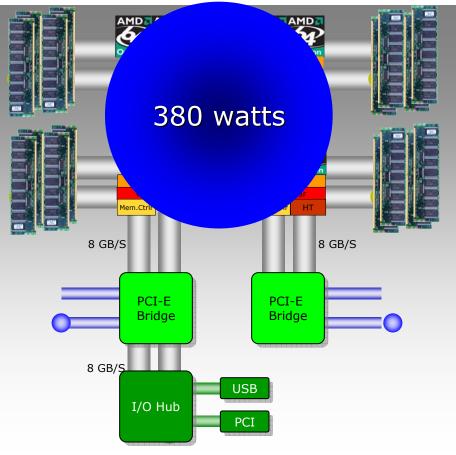
- 692 watts for processors (173w each)
- 48 watts for external memory controller

**\$1037** per/year (1 server)

**\$518,592** per/year (500 servers)

95% More

740 watts



#### שעמו-טטו ב אואוש טאנבוטוו אוטעבאטטו א

- 380 watts for processors (only 95w each)
- Integrated memory controllers

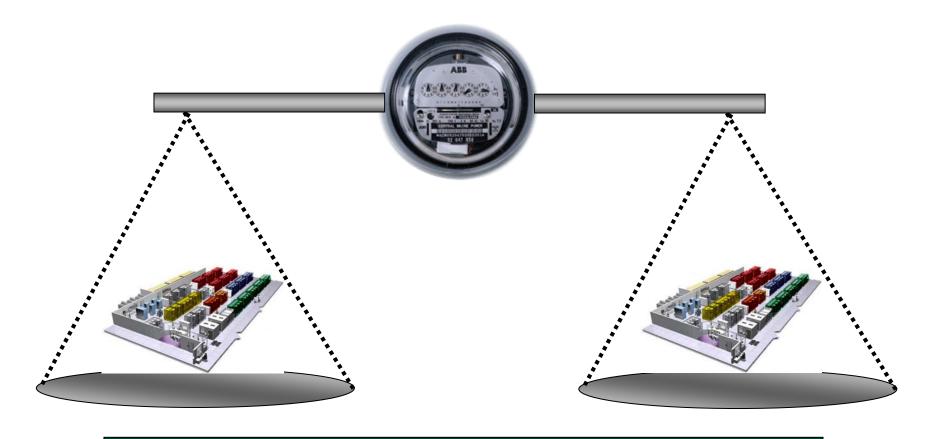
\$533 per/year (1 server)

\$266,304 per/year (500 servers)

380 watts



### It takes a "Balanced" Architecture

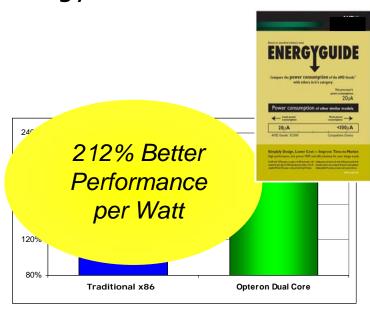


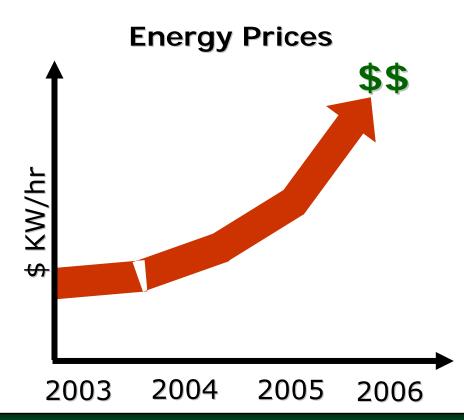
It takes a "Balanced" Microprocessor Architecture to maintain a "Balanced" Datacenter



## **Industry Developed Metrics Enabling Energy Efficient Datacenters**

 Customers are asking for energy efficient metrics





AMD Challenges the Industry to work together to develop a energy efficiency metric



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